## ABSTRACT OF THE DISCLOSURE

A ferroelectric memory according to the present invention includes a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged, and a peripheral circuit for the passive matrix array. The passive matrix array is formed of a passive matrix array microchip, and the peripheral circuit, such as a word line driver circuit or a bit line driver circuit, is formed on a peripheral circuit substrate, thereby integrating the passive matrix array microchip on the peripheral circuit substrate. Since this structure allows the passive matrix array and the peripheral circuit therefor to be separately fabricated, the peripheral circuit is not adversely affected when fabricating the passive matrix array, thereby decreasing the degree of limitation in the fabrication process.

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